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ABSTRACT

An integrated circuit is provided with high-aspect ratio vias in which the upper channel after lining with an adhesion/barrier layer is used as a collimator with a via entrant angle of greater than about 70 degrees during the ionized metal plasma deposition of the seed layer over the adhesion/barrier layer. This results in a seed layer with reduced overhang in the vias enhancing the subsequent filling of the vias by a conductive layer and preventing the formation of voids in the vias.